

REMARKS

The following remarks are fully and completely responsive to the Office Action dated April 12, 2004. Claims 4-10 are pending in this application. By this Amendment, claim 4 has been amended. In the outstanding Office Action, claims 4, 5, 7 and 9 were rejected under 35 U.S.C. §102(e) and claims 6, 8 and 10 were rejected under 35 U.S.C. §103(a). No new matter has been added. Claims 4-10 are presented for reconsideration.

Specification

At paragraph 2 on page 2, the Office Action notes that page 5, line 26 of the specification may have a typo. This paragraph at page 5, lines 23-27 of the specification has been amended to correct the typo identified by the Office Action.

35 U.S.C. § 102(e)

Claims 4, 5, 7 and 9 were rejected under 35 U.S.C. §102(e) as being anticipated by Haraguchi (U.S. Patent No. 6,178,127 B1). In making this rejection, the Office Action asserts that this reference teaches each and every element of the claimed invention. Applicants respectfully submit that claims 4, 5, 7 and 9 recite subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 4, as amended, recites a semiconductor memory device having at least the elements of a "redundant circuit" that "includes a storage circuit for storing the information supplied from the defective line information store circuit, and makes the substitution on the basis of the information stored in the storage circuit" in addition to a

"defective line information store circuit for storing information showing defective lines in a plurality of subblocks according to subblocks." In other words, a defective line information store circuit stores information showing defective lines. The defective line information store circuit supplies the information to a storage circuit in a redundant circuit. The redundant circuit makes a substitution on the basis of the information stored in the storage circuit. As such, the present invention of claim 4 results in the advantages of simple structure and operation of a semiconductor memory device.

It is respectfully submitted that the prior art fails to disclose or suggest each and every element of Applicants' invention as set forth in claim 4, as amended, and therefore fails to provide the advantages that are provided by the present application.

Haraguchi discloses a semiconductor memory device including a redundant column for repairing a defective memory cell column by replacement. The semiconductor memory device of Haraguchi has "replacement IO program circuits RIP1-RIPn" that store information designating the internal data line pair to be connected to a redundant column. This device of Haraguchi also has "replacement column address program circuits RAP1-RAPn" that store a defective column address designating a defective column to be repaired (column 2, lines 7-23). Thus, in Haraguchi, the "replacement IO program circuits RIP1-RIPn" and the "replacement column address program circuits RAP1-RAPn" store different kind of information from each other. Information stored in the "replacement IO program circuits RIP1-RIPn" is not supplied to the "replacement column address program circuits RAP1-RAPn", and information stored in the "replacement column address program circuits RAP1-RAPn" is not supplied to the "replacement IO program circuits RIP1-RIPn".

Therefore, Haraguchi fails to disclose or suggest at least the “redundant circuit” that “includes a storage circuit for storing the information supplied from the defective line information store circuit, and makes the substitution on the basis of the information stored in the storage circuit” as recited in claim 4, as amended. Accordingly, Applicants respectfully submit that Haraguchi fails to disclose or suggest each and every element recited in claim 4 of the present invention, and therefore claim 4 is allowable.

As claim 4 is allowable, Applicants submit that claims 5, 7 and 9, depending from allowable claim 4, are likewise allowable over the cited prior art. Consequently, Applicants request reconsideration and withdrawal of the rejection of claims 4, 5, 7 and 9 under 35 U.S.C. §102(e).

35 U.S.C. § 103(a)

Claims 6, 8 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Haraguchi. In making this rejection, the Office Action asserts that this reference teaches each and every element of the claimed invention.

Applicants respectfully submit that claims 6, 8 and 10 are dependent from claim 4. As such, claims 6, 8 and 10 are allowable due to their dependency on claim 4, which is allowable for reasons discussed above. Therefore, Applicants request reconsideration and withdrawal of the rejection of claims 6, 8 and 10 under 35 U.S.C. §103(a).

Conclusion

Applicants' amendments and remarks have addressed the typo in the specification and overcome the rejections set forth in the Office Action dated April 12, 2004. Applicants' amendment to the specification corrects the typo noted in the Office Action. Applicants' remarks have distinguished claims 4-10 from Haraguchi and, thus overcome the rejections of these claims under 35 U.S.C. §102(e) and §103(a). Accordingly, claims 4-10 are in condition for allowance. Therefore, Applicants respectfully request reconsideration and allowance of claims 4-10.

Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicants hereby petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 107337-00053.

Respectfully submitted,
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Enclosure: Petition for Extension of Time

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